

ESTEREL on FPGA via ECLAT (WIP)

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Compilation scheme for ESTEREL in the ECLAT compiler

$$\left(\begin{array}{c} \boxed{e} \end{array} \right)_{\rho, \alpha}^{\ell, x} = \begin{array}{l} \text{case state}_{\ell} \text{ is} \\ \text{when enum}(\text{IDLE}_{\ell}) \Rightarrow \boxed{\text{rdy}_{\ell} := \text{false}} ; \boxed{S} \\ \boxed{t_1 \cdots t_n} \\ \text{end} \end{array}$$

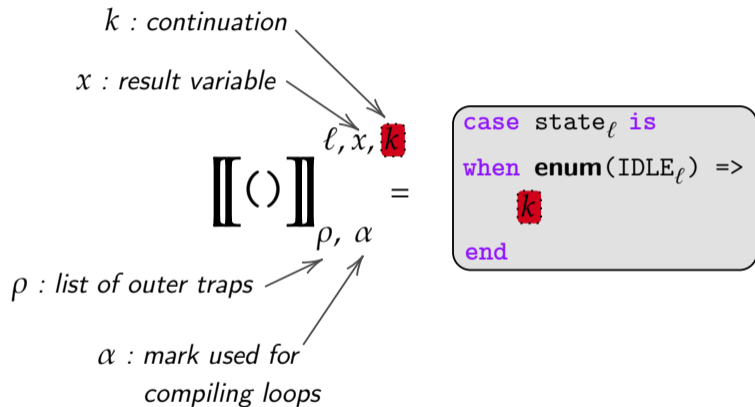
where $\left\{ \begin{array}{l} \left[\begin{array}{c} \boxed{e} \end{array} \right]_{\rho, \alpha}^{\ell, x, \boxed{k}} = \begin{array}{l} \text{case state}_{\ell} \text{ is} \\ \text{when enum}(\text{IDLE}_{\ell}) \Rightarrow \boxed{S} \\ \boxed{t_1 \cdots t_n} \\ \text{end} \\ \boxed{k} = (\boxed{\text{rdy}_{\ell} := \text{true}} ; \text{state}_{\ell} := \text{enum}(\text{IDLE}_{\ell})) \end{array} \right.$

naming convention:

- ℓ (id of the current FSM)
- state_{ℓ} (state variable)
- IDLE_{ℓ} (initial state)
- rdy_{ℓ} (when result is rdy)

invariant: once rdy_{ℓ} is true, the FSM reenters in the initial state $\text{enum}(\text{IDLE}_{\ell})$ at the next instant

Compiling “nothing”



Compiling valued signals

$\llbracket \text{emit } y(a) \rrbracket_{\rho, \alpha}^{\ell, x, k} =$

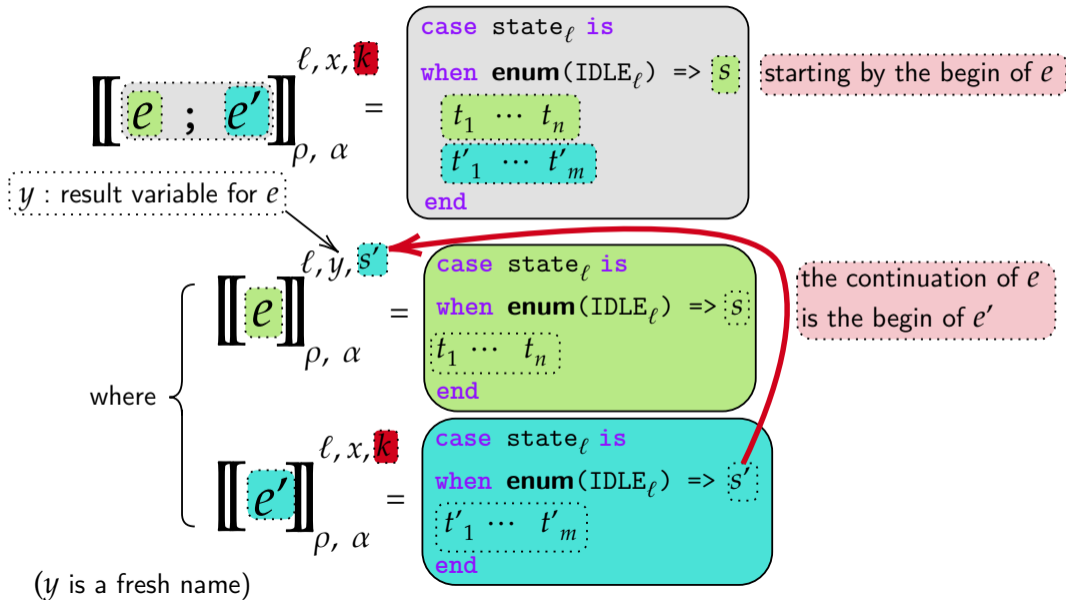
```
case stateℓ is
when enum(IDLEℓ) =>
  y <= a ; k
end
```

x : result variable

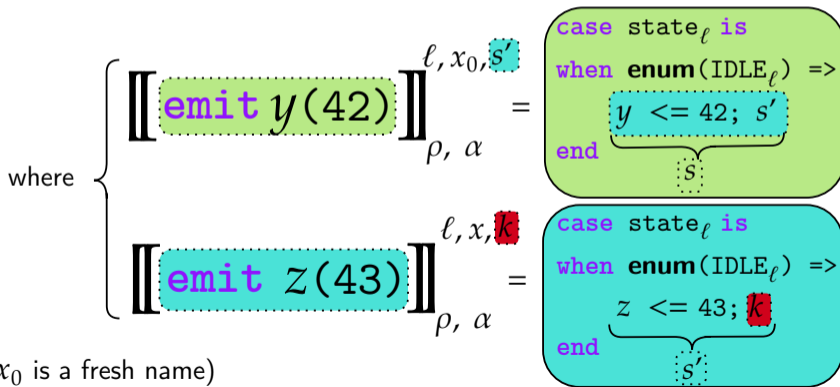
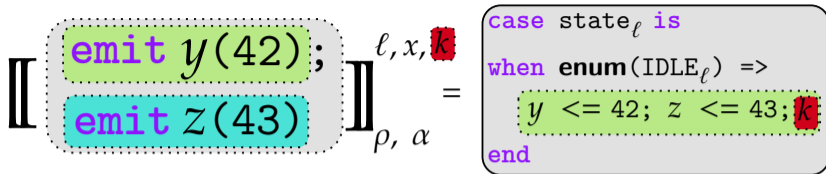
$\llbracket ?y \rrbracket_{\rho, \alpha}^{\ell, x, k} =$

```
case stateℓ is
when enum(IDLEℓ) =>
  x := ?y ; k
end
```

Compiling sequences



Example



Compiling conditionals

$\llbracket \text{if } a \text{ then } e \text{ else } e' \rrbracket_{\rho, \alpha}^{\ell, x, k}$

```

case stateℓ is
when enum(IDLEℓ) =>
  if a then s else s'
  t1 ... tn t'1 ... t'm
end
  
```

where $\llbracket e \rrbracket_{\rho, \alpha}^{\ell, x, k}$

```

case stateℓ is
when enum(IDLEℓ) => s
  t1 ... tn
end
  
```

NB: in the general case, need to duplicate k

k is what remains to do in the instant, e.g.:
 (rdy_ℓ := true;
 state_ℓ := enum(IDLE_ℓ))

$\llbracket e' \rrbracket_{\rho, \alpha}^{\ell, x, k}$

```

case stateℓ is
when enum(IDLEℓ) => s'
  t'1 ... t'm
end
  
```

Local signals

$$\llbracket \text{signal } y \text{ in } e \rrbracket_{\rho, \alpha}^{\ell, x, k} = \llbracket e \rrbracket_{\rho, \alpha}^{\ell, x, k}$$

NB: assumes that name y is declared only once (renaming by the compiler)

Compiling `exit`

$\llbracket \text{exit } y \rrbracket_{\rho, \alpha}^{\ell, x, k} =$

```
case stateℓ is
when enum(IDLEℓ) =>
  y := true
end
```

note that $y \in \rho$

NB: the continuation k is cut

Compiling **traps**, using an internal state machine

$\llbracket \text{trap } y \text{ in } e \rrbracket_{\rho, \alpha}^{\ell, x, k} =$

where $\left(\left[e \right] \right)_{(y \cdot \rho), \alpha}^{L, x} =$

```

case stateL is
when enum(IDLEL) => s
t1 ... tn
end
    
```

(L and WAIT are fresh)

```

disjonction_traps(x1, ... xn)
:= x1 ∨ ... ∨ xn
    
```

```

case stateℓ is
when enum(IDLEℓ) =>
y := false ;
s ; (if disjonction_traps(ρ) then ()
     else if y ∨ rdyL then k
     else stateL := enum(WAIT) )
when enum(WAIT) =>
case stateL is
when enum(IDLEL) => () t1 ... tn
end ;
(if disjonction_traps(ρ) then ()
 else if y ∨ rdyL then k
 else stateL := enum(WAIT) )
end
    
```

internal state machine (with id L)

Compiling suspend

\llbracket suspend e when y $\rrbracket_{\rho, \alpha}^{\ell, x, k} =$

where $\left(\left(e \right) \right)_{\rho, \alpha}^{L, x} =$

```

case stateL is
when enum(IDLEL) => s
t1 ... tn
end
    
```

(L and $WAIT$ are fresh)

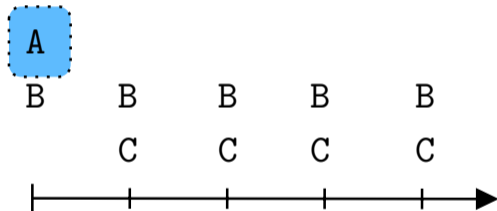
```

case stateℓ is
when enum(IDLEℓ) =>
( (s; if rdyL then k else stateℓ := enum(WAIT))
when enum(WAIT) =>
if ?y then stateℓ := enum(WAIT) else ((
case stateL is
when enum(IDLEL) => ()
t1 ... tn
end
)); if rdyL then k
else stateℓ := enum(WAIT))
end
    
```

internal state machine (with id L)

Loop in Esterel

```
emit A ;  
loop  
  emit B ;  
  pause ; emit C ;  
end ;  
emit D } dead code
```



Compiling loops

$\llbracket \text{loop } e \text{ end} \rrbracket_{\rho, \alpha}^{\ell, x, k}$

```

case stateℓ is
when enum(IDLEℓ) => s
  t1 ⋯ tn t'1 ⋯ t'm
end
  
```

```

α ::=
| 1 (not the end
   of a loop)
| 2 (end of loop)
  
```

inspired by Tardieu's approach for compiling loops

where $\llbracket e \rrbracket_{\rho, \max(\alpha, 1)}^{\ell, x, s'}$

```

case stateℓ is
when enum(IDLEℓ) => s
  t1 ⋯ tn
end
  
```

$\llbracket \text{rename}(e) \rrbracket_{\rho, 2}^{\ell, x, ()}$

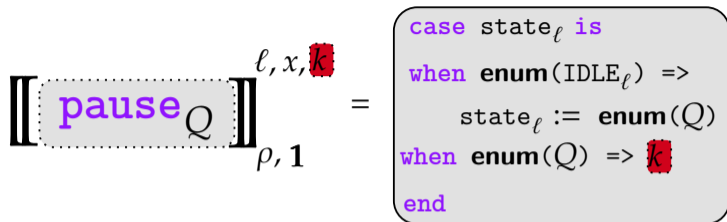
```

case stateℓ is
when enum(IDLEℓ) => s'
  t'1 ⋯ t'm
end
  
```

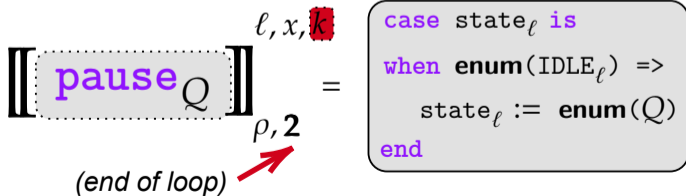
The continuation of the body is the start of the renamed body

reincarnation: renaming traps and signals

Compiling pauses

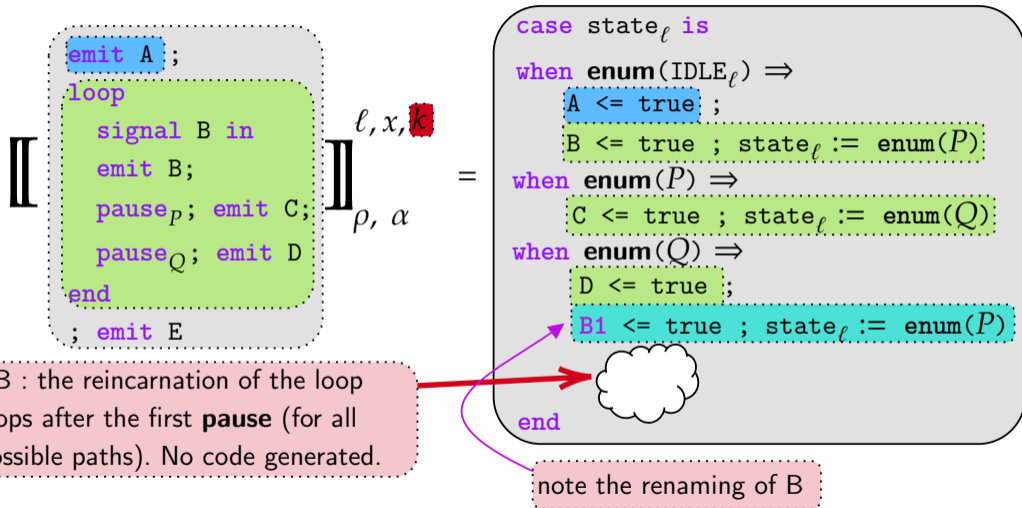


each pause is labeled with a unique name Q (not visible in source programs)
pause labels are not renamed when compiling loops, thus ensuring looping

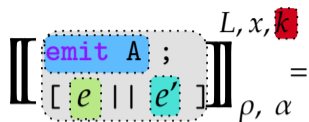


NB: the transition associated to Q already have been compiled in the first part of the current loop

Example of compilation



Parallel execution (1/3)



```

case stateL is
when enum(IDLEL) =>
  A <= true ;
  ( ( e ) )ℓ, yρ, α ;
  ( ( e' ) )ℓ', y'ρ, α ;
  if rdyℓ & rdyℓ' then x0 := (x, x') ; k ;
  else stateL := enum(IDLEL) ;
end
  
```

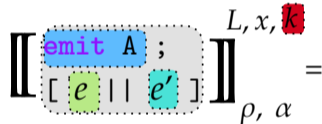
(reexecuting the past)

WRONG !

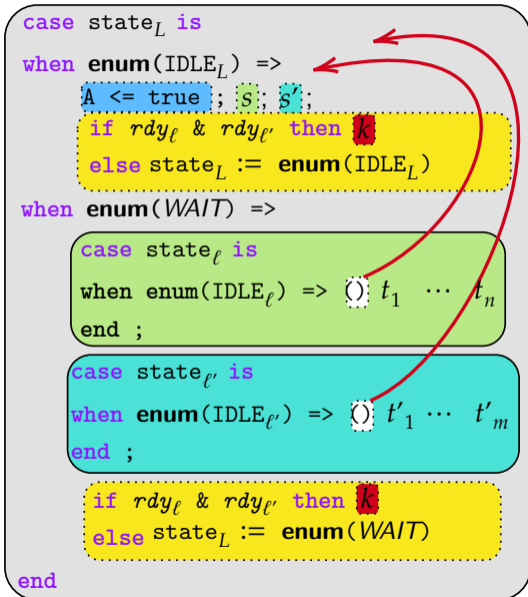
NB: by construction, each time rdy_ℓ [resp. rdy_{ℓ'}] is true, the FSM returns to state enum(IDLE_ℓ) [resp. enum(IDLE_{ℓ'})]

(ℓ, ℓ', y, y' are fresh)

Parallel execution (2/3)

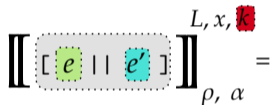


$(\ell, \ell', y, y', WAIT$ are fresh)



Parallel execution (3/3)

```
disjunction_traps( $x_1, \dots, x_n$ )
:=  $x_1 \vee \dots \vee x_n$ 
```



($\ell, \ell', y, y', WAIT$ are fresh)

```
case stateL is
when enum(IDLEL) =>
  S; S; if rdyℓ & rdyℓ' then
    (if disjunction_traps( $\rho$ ) then () else K)
    else stateL := enum(IDLEL)
when enum(WAIT) =>
  case stateℓ is
  when enum(IDLEℓ) => () t1 ... tn
  end ;
  case stateℓ' is
  when enum(IDLEℓ') => () t'1 ... t'm
  end ;
  if rdyℓ & rdyℓ' then
    (if disjunction_traps( $\rho$ ) then () else K)
    else stateL := enum(WAIT)
end
```